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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Hyun Joon SOHN**, a citizen of the Republic of Korea, residing at 891-10 Daechi-dong, Gangnam-gu, Seoul, Korea have invented a new and useful **SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING THE SAME**, of which the following is a specification.

SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING THE SAME

TECHNICAL FIELD

[0001] The present disclosure relates to semiconductors and, more particularly, to semiconductor devices and methods of manufacturing the same.

BACKGROUND

[0002] Recently, as semiconductor devices have become highly integrated, it is desirable to have excellent characteristics in a small area in processes for isolating unit elements. This requires a decrease in the number of defects, the use of a good quality gate oxide film, and a development of techniques for isolating the element.

[0003] FIGS. 1A to 1D illustrate cross sectional views sequentially showing a conventional process of fabricating a semiconductor device. As shown in the drawings, after a hard mask material is coated on a wafer 10 to form a hard mask layer 11, a photoresist pattern 12 is formed on the hard mask layer 11. Following the application of the photoresist pattern 12, a mask for forming a trench isolation is formed by a dry etching process.

[0004] Next, the photoresist pattern 12 is removed, and a trench isolation 14 is formed by another dry etching process. Thereafter, an oxide film (not shown) is coated on the inside surface of the trench by an oxide film forming process.

[0005] The trench is then filled with a dielectric material, wherein the oxide film is coated thereon. By a Chemical Mechanical Polishing (CMP) process, an upper part of the dielectric material and the hard mask layer 11 are planarized until the hard mask layer 11 is removed. A cleaning process is then performed to eliminate entirely any hard mask material remaining on the wafer. Then, a well 17, a source region 15 and a drain region 16 are formed by a photoresist process and an ion implantation process, and finally a gate oxide film is formed. At this time, by many processes performed previously, especially the cleaning process, a divot 19 is generated.

[0006] After a polysilicon layer is coated on the entire wafer, a gate 21 is formed by a photoresist process and a dry etching process.

[0007] However, in such fabricating method described above, a poly residue or poly stringer 20 is produced due to the divot 19. The presence of the poly stringer 20 deteriorates the operational characteristics and reliability of the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIGS. 1A to 1D illustrate cross sectional views sequentially showing a conventional method of fabricating a semiconductor device; and

[0009] FIGS. 2A to 2E depict cross sectional views sequentially showing a example method of fabricating a semiconductor device in accordance with one example disclosed herein.

DETAILED DESCRIPTION

[0010] Examples of the disclosed methods and devices will now be described in detail with reference to the accompanying drawings, wherein like reference numerals appearing in the drawings represent like parts.

[0011] As shown in FIGS. 2A to 2E, a source region 31, a drain region 32, and a well 33 are formed in a semiconductor wafer 30 by a photoresist process and an ion implantation process. After a cleaning process is performed, a gate oxide film 34 is formed on the wafer 30 (Fig. 2A).

[0012] A polysilicon film 35 is coated on the gate oxide film 34 and a first photoresist pattern 36 for forming a trench is formed on the polysilicon film 35 (Fig. 2B).

[0013] A trench isolation 38 may be formed in the wafer 30 by a dry etching process using the photoresist pattern 36 as a mask (Fig. 2C).

[0014] An oxide film is coated on the inside surface of the trench isolation 38, and a dielectric material 40 is provided to fill in the trench isolation 38. The dielectric material 40 is then planarized to expose the top surface of the polysilicon film 35 by a CMP process (Fig. 2D).

[0015] A second photoresist pattern 37 is formed on the polysilicon film 35 by a photoresist process and a gate 41 is formed by dry etching the polysilicon film 35 using the second photoresist pattern 37 as a mask (Fig. 2E).

[0016] The gate 41 is formed by a two-step dry etching process including a first etching process without any selective ratio to the dielectric material, and a second etching process with a selective ratio to the dielectric material; and, therefore, the dielectric material 40 in the trench isolation 38 is not protruded from the gate oxide film 34.

[0017] According to the disclosed example methods described above, there is provided a semiconductor device including the well 33, the source region 31 and the drain region 32 formed in the semiconductor wafer 30, the gate oxide film 34 formed on the wafer, the gate 41 formed on the gate oxide film, and the trench isolation 38 in which the dielectric material is filled.

[0018] According to the present disclosure, the number of processes before the formation of the gate oxide film 34 is reduced and, therefore, a pitting phenomenon of the wafer 30 due to wafer damages and defects is decreased, thereby improving a reliability of the gate oxide film 34 and electrical and operational characteristics of the device.

[0019] Further, no divot is formed at the edge of the trench so that a poly residue or poly stringer 20 is not produced, thereby increasing a reliability of the gate oxide film and decreasing defects to improve the operating characteristics of the semiconductor device.

[0020] Although certain apparatus and methods are disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers every apparatus, method, and article of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.